



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application of: Rajski et al.

Application No. 09/620,021

Filed: July 20, 2000

Confirmation No. 3823

For: CONTINUOUS APPLICATION AND
DECOMPRESSION OF TEST PATTERNS
TO A CIRCUIT-UNDER-TEST

Examiner: Phung M. Chung

Art Unit: 2133

Attorney Reference No. 1011-54375-01

COMMISSIONER FOR PATENTS
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Attorney or Agent
for Applicants *Law*Date Mailed 1.10.07INFORMATION DISCLOSURE STATEMENT PURSUANT TO
37 C.F.R. § 1.97(c)

Listed on the accompanying form PTO-1449 and enclosed herewith are several English-language and/or non-English-language documents. Among the documents are four English-language translations of portions of Japanese patent references previously disclosed. Additional copies of the original Japanese patent references are included with the translations. Applicants respectfully request that these documents be listed as references cited on the issued patent. This Information Disclosure Statement ("IDS") is being mailed before Applicants received a final action, a notice of allowance, or an action that otherwise closes prosecution in the referenced application.

Japanese Patent Publication No. 63-286780 describes a fault detecting system and fault detecting device. Japanese Patent Publication No. 03-012573 describes a logic circuit testing device having a test data changing circuit. Japanese Patent Publication No. 05-249197 describes an incorporated self-test circuit. Japanese Patent Publication No. 07-174822 describes a semiconductor integrated circuit device. Japanese Patent Publication No. 08-015382 describes a circuit incorporating a self test function. Japanese Patent Publication No. 11-264860 describes an output circuit of a semiconductor device with test mode.

Copies of United States patents and United States published patent applications do not have to be provided to the Patent Office (37 C.F.R. 1.98(a)(2)(ii)). Copies of unpublished U.S. applications do not have to be provided, as long as the application is available on PAIR, as this requirement of 37 C.F.R. § 1.98(a)(2)(iii) has been waived by the United States Patent and Trademark Office pursuant to the Official Gazette Notice on October 19, 2004 (1287 OG 163). Applicants will provide copies of such patents or applications upon request.

Submitted herewith is a check for \$180.00 as required by 37 C.F.R. § 1.17(p) for filing this IDS in compliance with 1.97(c).

Please charge any additional fees which may be required in connection with filing this IDS, or credit any overpayment, to Deposit Account No. 02-4550. A duplicate copy of this sheet is enclosed.

The filing of this IDS shall not be construed to be an admission that the information cited in the statement is, or is considered to be, prior art or otherwise material to patentability as defined in 37 C.F.R. §1.56.

Respectfully submitted,

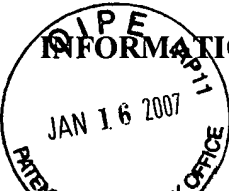
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Docketing

	Attorney Docket Number	1011-54375-01
	Application Number	09/620,021
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	First Named Inventor	Rajski
	Art Unit	2133
Examiner Name		Phung M. Chung

U.S. PATENT DOCUMENTS

Copies of U.S. Patent documents do not need to be provided, unless requested by the Patent and Trademark Office. For patents, provide the patent number and the issue date. For published U.S. applications, provide the publication number and the publication date. For unpublished pending patent applications, provide the application number and the filing date.

Examiner's Initials*	Cite No. (optional)	Number	Publication Date	Name of Applicant or Patentee
		5,072,178	12/10/1991	Matsumoto
		5,642,362	6/24/1997	Savir
		5,717,701	2/10/1998	Angelotti et al.
		6,467,058	10/15/2002	Chakradhar et al.
		6,590,929	7/8/2003	Williams
		6,763,488	7/13/2004	Whetsel

FOREIGN PATENT DOCUMENTS

Examiner's Initials*	Cite No. (optional)	Country	Number	Publication Date	Name of Applicant or Patentee
		Japan	63-286780 (w/partial translation)	11/24/1988	Iwasaki et al.
		Japan	03-012573 (w/English abstract)	1/21/1991	Matsumoto
		Japan	05-249197 (w/English abstract)	9/28/1993	Ikenaga et al.
		Japan	07-174822 (w/partial translation)	7/14/1995	Kondou
		Japan	08-015382 (w/partial translation)	1/19/1996	Hiraide et al.
		Europe	0 549 949	3/11/1998	Ikenaga et al.
		Japan	11-264860 (w/partial translation)	9/28/1999	Kitamura

OTHER DOCUMENTS

Examiner's Initials*	Cite No. (optional)	
		Konemann et al., "Built-In Logic Block Observation Techniques," <i>IEEE Test Conference</i> , 6 pp. (1979).

EXAMINER
SIGNATURE:

DATE
CONSIDERED:

* Examiner: Initial if reference considered, whether or not in conformance with MPEP 609. Draw line through cite if not in conformance and not considered. Include copy of this form with next communication to applicant.